REMARKS

Applicants respectfully request reconsideration and allowance of the subject application.

Claims 1-23 were originally submitted

Claim 14 was previously amended.

Claims 9 and 21 are currently amended.

Claims 24 and 25 were previously added.

No claims are canceled.

Claims 1-25 remain in this application.

35 U.S.C. §102

Claims 1, 4-11, 13-17, 21-25 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,085,333 to DeKoning et al (DeKoning). Reconsideration is requested.

Dependent claim 1 recites "[a] data array system for providing a host computer device having a host bus redundant access to a data storage device, comprising:

an active controller linked to the host bus and the data storage device, the active controller including a messaging mechanism for transmitting the messages and data over the host bus; and

a standby controller linked to the host bus and the data storage device, the standby controller including message and data buffers for storing the messages and data, whereby the host bus functions as an inter-controller-link.

DeKoning teaches a RAID storage subsystem 100, having redundant disk array controllers (RDAC) 118.1 and 118.2. One RDAC acts as primary controller and the other RDAC acts as a redundant controller. Each RDAC 118.1 and 118.2 is connected to a disk array 108 via bus (or busses) 150 and to host computer 120 via a separate bus 154. (DeKoning, col. 5 lines 14-23)

RDAC 118.1 includes a main CPU 112.1, a flash memory 114.3 and a program memory 114.1 for storing program instructions and variables for the operation of a CPU 112.1, a local memory 116.1 (i.e., cache memory) for storing data and control information related to the data stored in disk array 108, and a RAID Parity Assist (RPA) 113.1 memory. RDAC 118.1 also includes a co-processor 115.1 for controlling transfer of data to and from disk drives 110. Co-processor 115.1 is an inter-controller communication chip (ICON) application specific integrated circuit (ASIC) that provides communication and coordination for the transfer of data between the native controller's (i.e., RDAC 118.1) RPA memory 113.1 to the spare controller's (i.e., RDAC 118.2) RPA memory 113.2 without assistance of the CPU 112.1. In this case, the ICON ASIC (i.e., co-processor 115.1) executes application specific code which includes a set of address ranges to perform data transfers. CPU 112.1, flash memory 114.4, program memory 114.1, cache memory 116.1, and co-processor 115.1 are connected via memory bus 152.1 to enable CPU 112.1 to store and retrieve information in the memory devices 116.1, 114.1. (DeKoning col. 5 line 56 to col. 6 line 9)

RDAC 118.2 is identical to RDAC 118.1. RDAC 118.2 includes a CPU 112.2, a flash memory 114.4, a program memory 114.2, a cache memory 116.2, RPA memory 113.2, and a co-processor 115.2, all interconnected via memory bus

152.2. To permit each RDAC to communicate with the other, the RDACs 118.1 and 118.2 are interconnected via a shared bus 156. (DeKoning col. 6 lines 54-59)

Claim 1 recites in part "an active controller linked to the host bus and the data storage device, the active controller including a messaging mechanism for transmitting the messages and data over the host bus".

The Action presents that either RDAC 118.1 or 118.2 as an active controller that is linked to the host bus 154. The Action further presents that the CPU and co-processor of RDAC 118.1 or 118.2 as a messaging mechanism. As discussed, the CPUs communicate to their respective co-processors via a memory bus (e.g., bus 152.1 and 152.2). The co-processors are used to communicate transfer of data between one another's RPA memories. The co-processors are interconnected via a shared bus 156. The messaging is not over the host bus 154, but through the separate and distinct shared bus 156. Therefore, DeKoning fails to teach the element "a messaging mechanism for transmitting the messages over the host bus".

Claim 1 further recites "a standby controller linked to the host bus and the data storage device, the standby controller including message and data buffers for storing the messages and data, whereby the host bus functions as an inter-controller-link".

The Action presents that bus 154 of DeKoning functions as an "inter-controller link"; however, DeKoning teaches otherwise. As discussed above, the RDACs 118.1 and 118.2 communicate with one another over the separate and distinct shared bus 156, not over bus 154. Therefore, DeKoning fails to teach the element "the host bus functions as an inter-controller-link".

Accordingly, DeKoning does not show every element of claim 1, and the rejection of claim 1 is therefore improper. Accordingly, Applicant respectfully requests that the §102 rejection of claim 1 be withdrawn.

Claims 4-8 are allowable based at the least on their dependency on claim 1. Accordingly, Applicants respectfully request that the §102 rejection of claims 4-8 be withdrawn.

Independent claim 9 recites in part "with the active controller, transferring the message to the standby controller via the host bus".

As discussed above, DeKoning teaches that the RDACs 118.1 and 118.2 communicate with one another over the separate and distinct shared bus 156, not over bus 154. DeKoning does not teach "transferring the message to the standby controller via the host bus" as recited in claim 9.

Accordingly, DeKoning does not show every element of claim 9, and the rejection of claim 9 is therefore improper. Accordingly, Applicant respectfully requests that the §102 rejection of claim 1 be withdrawn.

Claims 10, 11 and 13 are allowable based at the least on their dependency on claim 9. Accordingly, Applicants respectfully request that the §102 rejection of claims 10, 11 and 13 be withdrawn.

Independent claim 14 recites in part "a host bus communicatively linking the host processor, the active controller, and the standby controller, wherein the active and standby controllers include redundancy messaging mechanisms configured to assert and sample signals on the host bus to provide inter-controller communications over the host bus".

As discussed above, RDACs 118.1 and 118.2 are linked with one another communicate with one another over the separate and distinct shared bus 156, not

bus 154. Therefore, DeKoning does not teach inter-controller communications over the host bus (i.e., bus 154) as recited in claim 14.

Accordingly, DeKoning does not show every element of claim 14, and the rejection of claim 14 is therefore improper. Accordingly, Applicant respectfully requests that the §102 rejection of claim 14 be withdrawn.

Claims 15-17 are allowable based at the least on their dependency on claim 14. Accordingly, Applicants respectfully request that the §102 rejection of claims 15-17 be withdrawn.

Independent claim 21 recites in part "with the active controller, writing data via the host bus to the interrupt range of the standby controller".

As discussed above, DeKoning teaches that the RDACs 118.1 and 118.2 communicate with one another over the separate and distinct shared bus 156, not over bus 154. Therefore, there is no teaching in DeKoning as to "writing data via the host bus to the interrupt range of the standby controller" as recited in claim 21.

Accordingly, DeKoning does not show every element of claim 21, and the rejection of claim 21 is therefore improper. Accordingly, Applicant respectfully requests that the §102 rejection of claim 21 be withdrawn.

Claims 22 and 23 are allowable based at the least on their dependency on claim 21. Accordingly, Applicants respectfully request that the §102 rejection of claims 22 and 23 be withdrawn.

Independent claim 24 recites in part "an active controller linked to the host bus and the at least one data storage device, the active controller including a messaging mechanism for transmitting the messages and data over the host bus; and, a standby controller linked to the host bus and the at least one data storage device, the standby controller including message and data buffers for storing the messages and data, whereby the host bus functions as an inter-controller-link configured to transfer data and message information between the active and standby controllers and wherein upon a failure of the active controller the inter-controller-link provides both data and message transfer within the computing device such that the host CPU can cause the standby controller to access data from the at least one data storage device".

The Action presents that the CPU and/or co-processor of RDACs 118.1 or 118.2 as a messaging mechanism that transmits over a host bus or bus 154; however, as discussed above the CPU and/or co-processor do not transmit over bus 154. Therefore, DeKoning does not teach the element "a messaging mechanism for transmitting the messages and data over the host bus" as recited by claim 24.

Furthermore, as discussed above, bus 154 taught in DeKoning is not an inter-controller-link between RDACs 118.1 and 118. In particular, DeKoning does not teach that the bus 154 may be an inter-controller-link that transfers data between the active and standby controllers as recited in claim 24. Contrary to what is presented in the Action, there is no teaching in DeKoning that bus 154 acting as a inter-controller-link provides both data and message transfer within the computing device such that the host CPU can cause the standby controller to access data from the at least one data storage device, as recited in claim 24. The

Action looks to DeKoning col. 6 line 60 to col. 7 line 39 as teaching this element. However, what is taught in this cited section of DeKoning is a redundant controller design. No teaching is made as to the use of bus 154 in performing the particular element of claim 24.

Accordingly, DeKoning does not show every element of claim 24, and the rejection of claim 24 is therefore improper. Accordingly, Applicant respectfully requests that the §102 rejection of claim 24 be withdrawn.

Independent claim 25 recites in part "an active controller sub-system linked directly to the host bus and the data storage device, the active controller sub-system including a messaging mechanism for transmitting messages and data over the host bus; and, a standby controller sub-system linked directly to the host bus and the data storage device, the standby controller sub-system including message and data buffers for storing the messages and data, whereby the host bus functions as a redundant inter-controller-link such that upon failure of either of the active controller subsystem and the standby controller sub-system the host computing device maintains access to the data storage device".

Similar arguments are presented by the Action in rejecting claim 25 as to rejecting claim 24. Applicants present arguments in support of claim 25 used in support of claim 24. In particular, Applicants present that DeKoning does not teach "a messaging mechanism for transmitting messages and data over the host bus" and "the host bus functions as a redundant inter-controller-link such that upon failure of either of the active controller subsystem and the standby controller sub-system the host computing device maintains access to the data storage device" as recited in claim 25.

Accordingly, DeKoning does not show every element of claim 25, and the rejection of claim 25 is therefore improper. Accordingly, Applicant respectfully requests that the §102 rejection of claim 25 be withdrawn.

35 U.S.C. §103

Claims 2-3 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeKoning in view of U.S. Patent No. 6,094,699 to Surugucchi et al. (Surugucchi). Reconsideration is requested.

Claims 2-3 depend from claim 1, and therefore include the elements of "an active controller linked to the host bus and the data storage device, the active controller including a messaging mechanism for transmitting the messages and data over the host bus" and "a standby controller linked to the host bus and the data storage device, the standby controller including message and data buffers for storing the messages and data, whereby the host bus functions as an inter-controller-link".

The Action relies on the arguments as to claim 1, relying on DeKoning. However, as discussed above in support of claim 1, DeKoning fails to teach the elements of claim 1.

Surugucchi is cited for teaching "PCI bus connecting PCI-compliant RAID controllers (col. 1 lines 19-27)"; however, Surugucchi provides no assistance in light of DeKoning as to the recited methodology of claim 1. Accordingly, a combination of DeKoning and Surugucchi fails to teach or suggest every element of claims 2-3, and the rejection of claims 2-3 is therefore improper. Applicants respectfully request that the §103 rejection of claims 2-3 be withdrawn.

Claim 20 depends on claim 14, and therefore includes the element "a host bus communicatively linking the host processor, the active controller, and the standby controller, wherein the active and standby controllers include redundancy messaging mechanisms configured to assert and sample signals on the host bus to provide inter-controller communications over the host bus".

The Action relies on the arguments as to claim 1 (claim 14), relying on DeKoning. However, as discussed above in support of claim 14, DeKoning fails to teach the particular element of claim 14.

Surugucchi is cited for teaching "PCI bus connecting PCI-compliant RAID controllers (col. 1 lines 19-27)"; however, Surugucchi provides no assistance in light of DeKoning as to the recited system of claim 14. Accordingly, a combination of DeKoning and Surugucchi fails to teach or suggest every element of claim 20, and the rejection of claim 20 is therefore improper. Applicants respectfully request that the §103 rejection of claim 20 be withdrawn.

Claim 12 is rejected under 35 U.S.C, 103(a) as being unpatentable over DeKoning in view of U.S. Patent 5,659,718 to Osman et al (Osman). Reconsideration is requested.

Claim 12 depends from claim 9, and therefore includes the element "with the active controller, transferring the message to the standby controller via the host bus".

The Action relies on the arguments as to claim 11, relying on DeKoning. However, as discussed above in support of claims 9 and 11, DeKoning fails to teach the elements of claims 9 and 11.

Osman is cited for teaching "message including information which defines the data as all or partial (a frame or a burst) (col. 12, lines 31-53)"; however,

Osman provides no assistance in light of DeKoning as to the recited method of claim 14. Accordingly, a combination of DeKoning and Osman fails to teach or suggest every element of claim 14, and the rejection of claim 14 is therefore improper. Applicants respectfully request that the §103 rejection of claim 14 be withdrawn.

Claims 18-19 is rejected under 35 U.S.C. 103(a) as being unpatentable over DeKoning in view of U.S. Patent No. 5,142,683 to Burkhardt, Jr. et al. (Burkhardt). Reconsideration is requested.

Claims 18-19 depend from claim 14, and therefore include the element "a host bus communicatively linking the host processor, the active controller, and the standby controller, wherein the active and standby controllers include redundancy messaging mechanisms configured to assert and sample signals on the host bus to provide inter-controller communications over the host bus".

The Action relies on the arguments as to claim 17, relying on DeKoning. However, as discussed above in support of claims 14 and 17, DeKoning fails to teach the elements of claims 14 and 17.

Burkhardt is cited for teaching "transmitting a signal (response available) to the source device (processor 29) upon completion of the transfer of the data out of the data buffer and transmitting an interrupt to the source device (col. 14, lines 57-68)"; however, Burkhardt provides no assistance in light of DeKoning as to the recited system of claims 18-19. Accordingly, a combination of DeKoning and Burkhardt fails to teach or suggest every element of claims 18-19, and the rejection of claims 18-19 is therefore improper. Applicants respectfully request that the §103 rejection of claim 18-19 be withdrawn.

The Office maintains and presents the following rejections in the previous Office Action of October 19, 2005. Applicants maintain their position presented in the response to the Office Action of October 19, 2004, and address the response to Arguments presented in the current Action. Reconsideration is requested.

Claims 1-3, 9, 13-14, 17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,606,683 to Mori (Mori) in view of U.S. Patent No. 6,151,641 to Herbert (Herbert).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mori in view of Herbert in view of Osman.

Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori in view of and Osman.

Claims 10-11 and 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori in view of Herbert, and further in view of Burkhardt.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mori in view of Herbert and Burkhardt, and further in view of Osman.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mori in view of Herbert in view of U.S. Patent No. 6,115,803 to Hayashi et al (Hayashi).

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mori in view of Herbert and Hayashi, and further in view of Burkhardt.

Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori in view of Herbert, and further in view of U.S. Patent No. 5,675,807 to Iswandhi et al (Iswandhi).

In regards to Applicants' Response to the Office Action of October 19, 2004 the current Action states that "Applicant's arguments filed 02-18-05 have been fully considered but they are not persuasive".

In particular, the Action states:

> as addressed by the Examiner in the previous Office Action, Mori does not explicitly disclose how the active and standby controllers linked to the host bus, therefore they could directly link to the host bus or indirectly link to host bus (e.g. through several buses before it reaches the host bus). Therefore, implementing each of the controllers to attach directly to the host bus reducing the number of buses for connecting. It is noted that only the teaching of "controller(s) that attach directly to the host system's bus" is brought in, this will not destroy the invention of Mori since the controllers of Mori still can communicate to each other and to the host in the way taught in Mori, the only difference now is that they are directly connected to the host bus, instead of going through a couple of buses before reaching the host bus.

The Examiner seemingly relies on personal knowledge without pointing to any specific teaching in Mori. Specifically, the Examiner merely contends that "Mori does not explicitly disclose how the active and standby controllers linked to the host bus, therefore they could directly link to the host bus or indirectly link to host bus (e.g. through several buses before it reaches the host bus)".

According to 37 CFR §1.104(d)(2), "[w]hen a rejection in an application is based on facts within the personal knowledge of an employee of the office, the data shall be as specific as possible, and the reference must be supported, when called for by the applicant, by the affidavit of such employee, and such affidavit shall be subject to contradiction or explanation by the affidavits of the applicant and other persons." If this rejection is maintained on a similar basis in a subsequent action, the applicant respectfully requests the Examiner to supply such

an affidavit to support this modification of Mori. Otherwise, and without additional support, it is respectfully submitted the Examiner's conclusion does not represent the conclusion of a person of ordinary skill at the time of invention.

The Office has not addressed Applicant's position as to Herbert, and particularly that Herbert fails to teach "redundant controllers that attach directly to the host system's PCI bus". Therefore, since Mori fails to teach a host bus that links controllers and Herbert fails to teach redundant controllers attaching directly to the host system's PCI bus, there would be no motivation to combine Mori and Herbert.

Accordingly, a combination of Mori and Herbert fails to teach or suggest every element of claims 1-23, and the rejection of claims 1-23 is therefore improper. Applicants respectfully request that the §103 rejection of claims 1-23 be withdrawn.

CONCLUSION

All pending claims 1-25 are in condition for allowance. Applicants respectfully request reconsideration and prompt issuance of the subject application. If any issues remain that prevent issuance of this application, the Examiner is urged to contact the undersigned attorney before issuing a subsequent Action.

Respectfully Submitted,

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